Fraunhofer EMFT

Capacitively Coupled Transmission Line Pulsing CC-TLP

A reproducible stress method in the ESD CDM-domain

CC-TLP probe above wafer (raised).
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Applications

The Charged Device Model (CDM) is the major root cause for ESD (Electrostatic Discharge) failures in a modern production and test environment. CDM stress testing is well established for product qualification. Although specified as CDM failure voltage, mainly the peak current and pulse duration determine the failure threshold.

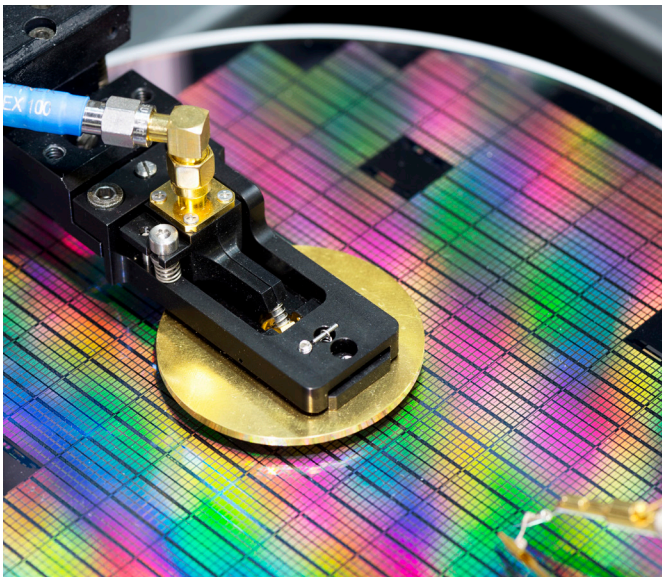
Devices returning damaged from the field frequently display an increased leakage current at the input due to a broken internal gate oxide behind the ESD protection. However, CDM severely lacks in repeatability and reproducibility over testers and time. Thus, an increasing demand arises for reliable stress and measurement techniques to decide up on costly redesigns and technology re-spins. Capacitively Coupled Transmission Line Pulsing CC-TLP, which was invented and developed at the Fraunhofer EMFT overcomes this drawback of standard CDM qualification tests by applying a CDM-like stress showing a very high reproducibility concerning the stress impulses. This allows precise determination of the failure threshold of a product, thus increasing the confidence in the results significantly.

Technical innovation

Transmission Line Pulsing (TLP) is a well established method for characterizing test structures or products in the ESD-relevant time

and current domains. Commercially available TLP testers trigger the test pulses in a relay and thus ensure a high repeatability and reproducibility of the rise time and pulse amplitude. However, unlike CDM, which is a one-pin-stress method, TLP requires two contacts to the device.

Thus, Fraunhofer EMFT developed a special capacitively coupled probe (CC-TLP) which injects the TLP stress pulse directly via one pin into the device under test (DUT). The ground return path is established by the capacitance, which builds up between the ground plane of the probe and the package of the device. This mimics exactly the situation in a conventional CDM tester without showing its drawbacks due to air discharge-related spark effects. Furthermore, the design of the probe allows stress tests at wafer level, which enables the access to CDM-relevant data at an earlier design stage without the need of packaging the DUT. In addition, this also allows the pre-characterization of dies as part of multichip modules (MCM) in order to ensure a sufficiently high ESD robustness of the complete system.



CC-TLP test at wafer level. ©Fraunhofer EMFT/Bernd Müller

Technical data

The CC-TLP probe was developed and the concept was proven in many studies together with semiconductor manufacturers. The signal bandwidth of the CC-TLP probe is higher than 20 GHz. The height of the ground plane which determines the capacitive coupling can be adjusted in a range between 100 µm and 1 mm.

A selection of studies and publications

J. Weber, R. Fung, R. Wong, H. Wolf, H. A. Gieser, L. Maurer
Stress current slew rate sensitivity of an ultra-highspeed interface IC
IEEE Transactions on Device and Materials Reliability, Vol. 19, Issue: 4, November 2019

H. Wolf, H. Gieser, W.Stadler, W. Wilkening,
Capacitively Coupled Transmission Line Pulsing CC-TLP – A Traceableand Reproducible Stress Method in the CDM-Domain
Journal of Microelectronics Reliability, Elsevier, volume 45, no. 2, 2005, pp. 279-285.

H. Wolf, H. Gieser, K. Bock, A. Jahanzeb, C. Duvvury, Y. Lin,
Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM
2009 31st EOS/ESD Symposium, Anaheim, USA, August 30-September 04, 2009

K. Esmark, R. Gaertner, S. Seidl, F. zur Nieden, H. Wolf, H. Gieser,
Using CC-TLP to get a CDM Robustness Value
2015 37th EOS/ESD Symposium, Reno, USA, September 27-October 02, 2015

Standardization

The standardization body of the ESD Association has published the standard practice document ANSI/ESD SP5.3.4-2022, which establishes the CC-TLP as an approved test method.

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